REMARKS/ARGUMENTS

The rejections presented in the Office Action dated February 21, 2007 (hereinafter Office Action) have been considered. Claims 1-19 remain pending in the application. Reconsideration of the pending claims and allowance of the application in view of the present response is respectfully requested.

Claims 8 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant acknowledges the indication of conditionally allowable subject matter.

Claims 1-7 and 9-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,987,554 to Liu et al. (hereinafter "*Liu*"). Applicant respectfully traverses the rejection. Applicant submits that *Liu* fails to expressly or inherently disclose all of the limitations of Claims 1-7 and 9-16.

In the rejection of independent Claims 1 and 10, column 6, lines 51-67 of *Liu* is relied upon to show a message-generating module that forms a report message having as leading bits thereof a report message header specified by the query data field in the report query message signal. *Liu* is also relied upon to show first and second nodes that send data on a shared serial data path, each providing an identical report message header responsive to a particular query data field value and series of lower order bits represent the node data value in the data signal generated by the node involved. Applicants respectfully submit that *Liu* fails to expressly or inherently teach or suggest at least these limitations of Claims 1-7 and 10-16.

The Office Action cites column 6, lines 51-67 of *Liu* to show a message-generating module that forms a report message having as leading bits a report message header, and where first and second nodes send data on a shared serial data path, each providing an identical report message header. The Office Action states that "response buffer 205 queues outgoing response data [as] they are received. The outgoing response data format is identical (identical report message header) with corresponding data as dictated from CPU A controller 03 109 (first node) and CPU B controller 04 111 (second node)." (Office Action,

page 3, lines 3-5). However, the Applicants note that the CPU controllers 109, 111 shown in FIG. 1 are coupled by an Inter-IC (I^2C) control bus, which *Liu* describes as "a bidirectional two-wire bus (a serial data line and a serial clock line)." (*Liu*, col. 1, lines 66-67) While not acquiescing that the I^2C can be characterized as a serial data path as set forth in independent Claims 1 and 10, Applicant nonetheless points out that the response buffer 205 relied upon in FIG. 2 is not part of a serial data path that couples the CPU controllers 109, 111. In *Liu's* FIG. 2, the response buffer 205 is part of the system interface 105 that couples the I^2C bus and ISA bus 103. In particular, the buffer 205 couples the system interface processor 201 to the ISA bus 103. Therefore the buffer 205 communicates directly on the ISA bus 103 and is separated from the I^2C bus by the processor 201.

The ISA bus is a parallel bus and not a serial data path as set forth in Applicant's claims (*see, e.g., Liu* FIG 3B, where FIFOs 303, 305 have eight data lines coupled to ISA bus 103). Therefore, any teachings in *Liu* related to the buffer 205 are irrelevant to the I^2C bus because the buffer 205 does not transmit onto the I^2C bus. Further, Applicant is unable to find mention in *Liu* of any messages on the I^2C bus or ISA bus having identical report message headers. As such, Applicant respectfully submits that *Liu* fails to expressly or inherently show a message-generating module that forms a report message having as leading bits a report message header, and where first and second nodes send data on a shared serial data path, each providing an identical report message header.

For similar reason, Applicants submit that column 7, lines 51-52 and FIGS 1 and 2 of *Liu* fail to show a message-synchronizing module providing a synchronizing signal on the data path. According to the Office Action, this is taught in *Liu* because "the system interface commands 105 are executed synchronously." (Office Action, p. 3, lines 7-8). However, *Liu* does not show a synchronizing signal being applied to a shared serial data path. First, the portion of *Liu* that is relied to teach this feature (col. 7, lines 5-52) discusses access to the ISA bus using synchronous I/O. As *Liu* explains, asynchronous I/O mode uses processor interrupts to determine when I/O is complete, but synchronous I/O does not rely in interrupts. Instead, in synchronous I/O mode, a client polls a status to confirm command completion. (*Liu*, col. 7, lines 16-20 and 51-54). Thus *Liu* does not

describe a synchronizing signal being sent on a data path, because *Liu's* "synchronization" is related to external polling of I/O status and not to transmission of a synchronization signal on a data line. Further, *Liu's* description of the I^2C bus as having "a serial data line and a serial clock line" would not show a synchronizing signal being sent on a data path, because I^2C uses a clock line that is separate from the data line. (*Liu*, col. 1, lines 66-67). Thus, Applicants submit that *Liu* fails to expressly or inherently show a message-synchronizing module providing a synchronizing signal on the data path.

The Office Action further relies on the description of a request buffer 203 to show a message selection module that copies an assembled message into a send register and, responsive to a synchronizing signal, providing the send signal to the message-sending module. As with the response buffer 205, the request buffer 203 is a parallel buffer of the ISA bus, and the Applicant submits that the buffer 203 cannot be relied upon to teach the send registers coupled to a serial bus described in Claims 1 and 10. As a result, Applicants respectfully submit that *Liu* does not expressly or inherently disclose all of the features of Claims 1 and 10, and therefore these claims are allowable over *Liu*. Further, Claims 2-7 and 11-16 depend from Claims 1 and 10, respectively, and therefore Claims 2-7 and 11-16 are also allowable over *Liu* for the same reasons.

The above discussion presented in connection with the previously cited prior art merely sets forth reasons as to why the rationale presented in the Office Action would not be relevant to the presently claimed invention. No amendments have been made to the claims with respect to cited references, and new claims 18 and 19 have been added to further characterize alternative aspects of the present application. New claims 18 and 19 merely manifest Applicant's "long-accepted right to press alternative claims covering different aspects of ... [Applicant's disclosed] invention." *Amgen, Inc. v. Hoechst Marion Roussel*, 126 F. Supp.2d 69 (D. Mass. 2001). Applicant respectfully submits that, by way of this Office Action Response, there is no intention to narrow, nor has the Applicant narrowed the breadth of the claims as originally filed through the explanatory comments provided herein. New Claims 18 and 19 incorporate some aspects of the invention as set

forth in conditionally allowable Claims 8 and 17, and for at least that reason are also believed to be patentable over the cited references.

Authorization is given to charge Deposit Account No. 50-3581 (HONY.033PA) any necessary fees for this filing. If the Examiner believes it necessary or helpful, the undersigned attorney of record invites the Examiner to contact the undersigned attorney to discuss any issues related to this case.

Respectfully submitted,

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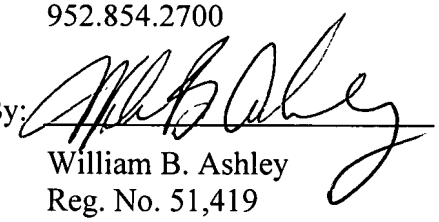
By: 

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